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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,121	01/22/2004	Hiroaki Nasu	9319S-000596	4193

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EXAMINER	
VILLECCO, JOHN M	
ART UNIT	PAPER NUMBER
2622	
MAIL DATE	DELIVERY MODE
05/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,121	NASU, HIROAKI	
	Examiner	Art Unit	
	JOHN M. VILLECCO	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 15, 2008 has been entered.

Response to Arguments

2. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. Please see the new grounds of rejection on the following pages.

3. Additionally, regarding claim 6, Official Notice was taken in the most recent Office Action regarding the use of a regulator for producing different voltages to be provided to the sensor. The Examiner's conclusion of common knowledge in the art is now taken to be admitted prior art because Applicant has failed to traverse the Examiner's assertion of Official Notice in reply to the Office Action in which the common knowledge statement was made. Please see MPEP § 2144.03.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuida (Japanese Publ. No. 2002-064749 A) in view of Yonemoto (Japanese Publ. No. 10-200817 A).

6. Regarding ***claim 1***, Mitsuida discloses a solid-state image pickup device which changes the gate applied voltage of a transistor in an imaging pixel. More specifically and as it relates to the applicant's claims. Mitsuida discloses a solid-state image pickup element (unit pixel, 101) including a photodiode (light-recieving diode 111) and one transistor (MOS transistor, 112) for detecting an optical signal and a circuit (drive scanning circuit, 102) for changing a gate applied voltage that changes a voltage applied to each gate of the transistors (see the abstract and paragraph 0050). The circuit (drive scanning circuit, 102) applies a predetermined voltage (ground) to each gate of a plurality of the transistors (all of the pixels) while in an accumulation state and another predetermined voltage (~2.2 V) while in a reading out state. See Figure 1 and paragraphs 0040 and 0045.

Mitsuida, however, fails to explicitly disclose that the voltages come from two different voltage sources. Yonemoto, however, discloses that it is well known in the art to apply different voltages from different sources to transistors. More specifically, Yonemoto discloses high (V_H), medium (V_M), and low (V_L) voltage sources for supplying different voltages to the transistors

(2). See Figures 5 and 2. While Mitsuida does discloses applying differing voltages (V_{pg}) to the transistor, he fails to specifically disclose how those differing voltages are supplied. Yonemoto's structure solves this problem. Therefore, it would have been obvious to one of ordinary skill in the art to include a voltage supplying circuit similar to Yonemotos' in the device of Mitsuida in order to supply the differing voltages from different voltage sources required by Mitsuida.

7. As for ***claim 2***, Mitsuida discloses a third predetermined voltage (See Figure 1) being applied to the gate electrode (19) of the transistor (112) during a clearing state (initialization). See paragraphs 0048-0049. In keeping with the obviousness rejection presented in claim 1, the third predetermined voltage would be supplied similarly to the circuit of Yonemoto

8. With regard to ***claim 3***, as shown in Figure 4 of Mitsuida, a plurality of gate voltage supplying circuits (the line from the drive scanning circuit to the gate electrode (19)) coupled to the gate (19) of the transistor (112). The changed applied voltage would be provided to the gate voltage supplying circuits (the line from the drive scanning circuit to the gate electrode (19)) from the circuit for changing the gate applied voltages (drive scanning circuit, 102).

9. Regarding ***claim 4***, as shown in Figure 4 of Mitsuida, a plurality of gate voltage supplying circuits (the line from the drive scanning circuit to the gate electrode (19)) coupled to the gate (19) of the transistor (112). It can be interpreted by the examiner that the lines from the drive scanning circuit (102) to the gate electrode (19) are part the circuit for changing the gate-applied voltage (drive scanning circuit, 102).

10. ***Claim 5*** is considered a method claim corresponding to claim 1. Please see a discussion of claim 1 on the preceding pages.

11. **Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuida (Japanese Publ. No. 2002-064749 A)**.

12. Regarding ***claim 6***, Mitsuida discloses a solid-state image pickup device which changes the gate applied voltage of a transistor in an imaging pixel. More specifically and as it relates to the applicant's claims. Mitsuida discloses a solid-state image pickup element (unit pixel, 101) including a photodiode (light-recieving diode 111) and one transistor (MOS transistor, 112) for detecting an optical signal and a circuit (drive scanning circuit, 102) for changing a gate applied voltage that changes a voltage applied to each gate of the transistors (see the abstract and paragraph 0050). The circuit (drive scanning circuit, 102) applies a predetermined voltage (ground) to each gate of a plurality of the transistors (all of the pixels) while in an accumulation state and another predetermined voltage (~2.2 V) while in a reading out state. See Figure 1 and paragraphs 0040 and 0045.

Mitsuida, however, fails to explicitly state the use of a regulator for producing the first and second voltages. Official Notice is taken that both the concept and the advantages of providing a regulator to provide different voltage values to different destinations from one source is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a regulator in the imaging device found in Mitsuida. as regulators are known to provide multiple different voltages as is required by the drive scanning circuit (102) of Mitsuida.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN M. VILLECCO whose telephone number is (571)272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN M. VILLECCO/
Primary Examiner, Art Unit 2622
May 23, 2008